Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Cancelled)
Claim 2 (Cancelled)
Claim 3 (Cancelled)
Claim 4 (Cancelled)
Claim 5 (Cancelled)
Claim 6 (Cancelled)
Claim 7 (Cancelled)
Claim 8 (Cancelled)
Claim 9 (Cancelled)
Claim 10 (Cancelled)
Claim 11 (Cancelled)
Claim 12 (Cancelled)
Claim 13 (Cancelled)
Claim 14 (Cancelled)
Claim 15 (Cancelled)
Claim 16 (Cancelled)
Claim 17 (Cancelled)
Claim 18 (Cancelled)
Claim 19 (Cancelled)
Claim 20 (Cancelled)
Claim 21 (Cancelled)
Claim 22 (Cancelled)
Claim 23 (Cancelled)
Claim 24 (Cancelled)
Claim 25 (Cancelled)
Claim 26 (Cancelled)
Claim 27 (Cancelled)
Claim 28 (Cancelled)

Claim 29 (New)
A content addressable memory device comprising:

rows of matchlines precharged to a voltage level corresponding to a miss condition,

a first number of ternary cells connected in parallel to each of the matchlines;

a second number of binary cells connected in parallel to each of the matchlines, the binary cells being smaller in size than the ternary cells and operable simultaneously with the ternary cells; and,

matchline sense amplifiers connected to each of the matchlines for detecting one of the miss condition and a match condition in response to search data, each matchline sense amplifier providing a match output if data stored in the ternary cells and the binary cells of each row matches the search data.

Claim 30 (New)
The content addressable memory device of claim 29, wherein the ternary cells include SRAM based ternary content addressable memory cells.

Claim 31 (New)
The content addressable memory device of claim 30, wherein the binary cells include SRAM based binary content addressable memory cells.

Claim 32 (New)
The content addressable memory device of claim 29, wherein the ternary cells include DRAM based ternary content addressable memory cells.

Claim 33 (New)
The content addressable memory device of claim 29, wherein the second number of binary cells are interleaved with the first number of ternary cells.

Claim 34 (New)
The content addressable memory device of claim 29, further including a third number of configurable ternary-binary content addressable memory cells connected in parallel to each of the matchlines.

Claim 35 (New)
The content addressable memory device of claim 29, wherein each of the rows of matchlines includes a segmented matchline.

Claim 36 (New)
The content addressable memory device of claim 35, wherein the segmented matchline includes a first matchline segment and a second matchline segment.

Claim 37 (New)
The content addressable memory device of claim 36, wherein the first number of ternary cells are coupled to the first matchline segment and the second number of binary cells are coupled to the second matchline segment.

Claim 38 (New)
The content addressable memory device of claim 29, wherein the first number is selected to store at least a corresponding number of header bits.

Claim 39 (New)
A content addressable memory device comprising:

rows of first matchlines precharged to a voltage level corresponding to a miss condition;

ternary cells connected in parallel to each of the first matchlines;

rows of second matchlines precharged to the voltage level corresponding to the miss condition;

binary cells connected in parallel to each of the second matchlines, the binary cells being smaller in size than the ternary cells and operable simultaneously with the ternary cells;

searchlines connected to the ternary cells of the rows of first matchlines and to the binary cells of the rows of second matchlines.

matchline sense amplifiers connected to each of the first matchlines and the second matchlines for detecting one of the miss condition and a match condition in response to search data on the searchlines, each matchline sense amplifier providing a match output if data stored in the ternary cells and the binary cells of each row matches the search data.

Claim 40 (New)
The content addressable memory device of claim 39, wherein the rows of first matchlines are interleaved with the rows of second matchlines.

Claim 41 (New)
The content addressable memory device of claim 39, wherein one row of first matchlines is adjacent to at least two consecutive rows of second matchlines.

Claim 42 (New)
The content addressable memory device of claim 39, wherein the ternary cells include DRAM based ternary content addressable memory cells and the binary cells include DRAM based binary content addressable memory cells.

Claim 43 (New)
A method for searching a content addressable memory array having rows of a first type of content addressable memory (CAM) cells and rows of a second type of CAM cells, the method comprising:
a) coupling search data specific to the first type of CAM cells to the first type of CAM cells and the second type of CAM cells;
b) disabling matchline sense circuits coupled to the rows of the second type of CAM cells; and
c) sensing matchlines corresponding to the rows of the first type of CAM cells in response to the search data.

Claim 44 (New)

The method of claim 43, wherein the first type of CAM cells include ternary CAM cells and the second type of CAM cells include binary CAM cells.

Claim 45(New)

The method of claim 44, wherein the ternary CAM cells include SRAM based ternary CAM cells.

Claim 46(New)

The method of claim 44, wherein the binary CAM cells include SRAM based binary CAM cells.

Claim 47(New)

The method of claim 44, wherein the ternary CAM cells include DRAM based ternary CAM cells.